

## CLAIMS

What is claimed is:

1. An electronic circuit for self-test of a random access memory array having a plurality of memory storage cells in a RAM circuit, wherein the storage cells are organized into a plurality of slice arrays, comprising:  
  
a control circuit;  
  
an address selection circuit, wherein the control circuit directs the address selection circuit to index through memory addresses;  
  
an input/output circuit associated with each slice array, wherein the control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address, to read data from the associated slice array at the indexed memory address, and to compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address; and  
  
an error detection circuit, wherein the error detection circuit collects results of the self-test data comparisons from each input/output circuit and notifies the control circuit of the results of the self-test.  
  
2. The electronic circuit as recited in claim 1, wherein the electronic circuit is embedded within the RAM circuit in an integrated circuit.  
  
3. The electronic circuit as recited in claim 1, wherein the control circuit and the address selection circuit are embedded in a control and address block of the RAM circuit.

- 2 4. The electronic circuit as recited in claim 1, wherein the control circuit  
4 initiates and terminates the self-test at preselected conditions, wherein the  
6 address selection circuit, informs the control circuit when the indexed  
memory address equals an initial self-test memory address, and wherein  
the address selection circuit, informs the control circuit when the indexed  
memory address equals a final self-test memory address.
- 2 5. The electronic circuit as recited in claim 1, wherein the address selection  
4 circuit comprises:  
6 an address multiplexer, wherein the address multiplexer has first, second,  
8 and third address-multiplexer inputs and an address-multiplexer output,  
10 wherein the second address-multiplexer input receives the memory  
12 address at which the self-test is initiated, wherein the third address-  
14 multiplexer input is configured to receive normal operational data  
16 addresses, and wherein when the address multiplexer receives command  
18 from the control circuit to initiate the self-test, the value of the second  
20 address-multiplexer input is transferred to the address-multiplexer output;  
22 a register, wherein the address-multiplexer output is connected to the  
input of the register and wherein the content of the register is used to  
address the RAM memory in writing and reading self-test data;  
a sequencer, wherein the output of the register is connected to the input  
of the sequencer, wherein the sequencer outputs an indexed version of the  
address received at the input of the sequencer, and wherein the output of  
the sequencer is connected to the first address-multiplexer input;  
a comparator, wherein the output of the register is connected to the input

24 of the comparator, wherein the comparator has first and second  
comparator outputs, wherein comparator first and second outputs are  
connected to the control circuit, wherein the first comparator output  
26 indicates when the register contains an initial self-test memory address,  
and wherein the second comparator output indicates when the register  
28 contains a final self-test memory address.

6. The electronic circuit as recited in claim 5, wherein the address  
2 multiplexer, the register, the sequencer, and the comparator are embedded  
in a control and address block of the RAM circuit.

7. The electronic circuit as recited in claim 1, wherein the input/output  
2 circuit comprises:

4 a data-in multiplexer, wherein the data-in multiplexer has first and second  
data-in-multiplexer inputs and a data-in-multiplexer output, wherein the  
6 first data-in-multiplexer input is configured to receive the self-test data,  
wherein the second data-in-multiplexer input is configured to receive  
8 normal operational data, and wherein:

10 when the data-in multiplexer receives command from the control  
circuit to perform the self-test, the value of the first data-in-  
12 multiplexer input is transferred to the data-in-multiplexer output,

14 otherwise, the second data-in-multiplexer input is configured to  
transfer its value to the data-in-multiplexer output;

16 an input register, wherein the output of the data-in-multiplexer output is  
18 connected to the input of the input register;

20 an inverter, wherein the output of the input register is connected to the  
input of the inverter;

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an input-complement multiplexer, wherein the input-complement  
24 multiplexer has first and second input-complement-multiplexer inputs and  
an input-complement-multiplexer output, wherein the output of the input  
26 register is connected to the first input-complement-multiplexer input,  
wherein the output of the inverter is connected to the second input-  
28 complement-multiplexer input, and wherein:

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when, the control circuit instructs the input-complement  
multiplexer to write test data into the slice array, the value of the  
32 first input-complement-multiplexer input is transferred to the  
input-complement-multiplexer output,

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otherwise, the value of the second input-complement-multiplexer  
36 input is transferred to the input-complement-multiplexer output;

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an output-complement multiplexer, wherein the output-complement  
multiplexer has first and second output-complement-multiplexer inputs  
40 and an output-complement-multiplexer output, wherein the output of the  
input register is connected to the first output-complement-multiplexer  
42 input, wherein the output of the inverter is connected to the second  
output-complement-multiplexer input, and wherein:

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when, the control circuit instructs the output-complement  
46 multiplexer to compare test data to data in the slice array, the  
value of the first output-complement-multiplexer input is  
48 transferred to the output-complement-multiplexer output,

50 otherwise, the value of the second output-complement-  
multiplexer input is transferred to the output-complement-  
52 multiplexer output;

54 an output register, wherein the output register receives the contents of the  
slice array; and

56 an exclusive-OR gate, wherein the exclusive-OR gate has first and second  
58 exclusive-OR-gate inputs and an exclusive-OR-gate output, wherein the  
output of the output register is connected to the first exclusive-OR-gate  
60 input, and wherein the output-complement-multiplexer output is  
connected to the second exclusive-OR-gate input.

8. The electronic circuit as recited in claim 7, wherein the input to the error  
2 detection circuit is connected to the exclusive-OR-gate output.